Abstract of the Disclosure

Microelectronic packages may be fabricated by forming a release layer on a process substrate. A thin film decal is formed on the release layer. The thin film decal includes first and second opposing decal faces, first decal input/output pads on the first decal face, second decal input/output pads on the second decal face and at least one internal wiring layer that electrically connects at least one of the first and second decal input/output pads. The first decal input/output pads are adjacent the release layer and the second decal input/output pads are remote from the release layer. A dielectric adhesive layer is then formed on the second decal face. The dielectric adhesive layer includes first and second opposing dielectric layer faces and conductive vias therein that extend between the first and second opposing dielectric adhesive layer faces. The first dielectric adhesive layer face is adjacent the second decal face and the second adhesive dielectric layer face is remote from the second decal face, such that at least one of the conductive vias electrically connects to at least one of the second decal input/output pads. The dielectric adhesive layer second face is then adhesively bonded to a second level substrate, such as a printed circuit board, that includes second level substrate input/output pads on a face thereof, such that at least one of the conductive vias electrically connects to at least one of the second level substrate input/output pads. The release layer is processed, for example dissolved, to thereby release the process substrate from on the first face of the thin film decal. A first level substrate, such as an integrated circuit chip, is then bonded to the first face of the thin film decal, for example by solder bump reflow.